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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/627,479  
Applicant : Kazushi Higashi et al.  
Filed : July 25, 2003  
Title : ELECTRONIC PART MOUNTING APPARATUS AND  
METHOD

Conf. No. : 4217  
TC/A.U. : 2835  
Examiner : TBD

Customer No. : 000,116  
Docket No. : 35955

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
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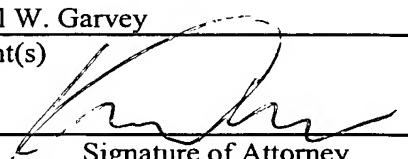
Sir/Madam:

In accordance with Rule 56, applicants are aware of the publications listed in the enclosed copy of Patent Office Form 1449. A copy of each of the publications is enclosed herewith. Translations and partial translations enclosed herewith were not prepared by, nor at the direction of, applicants or their assignees. Applicants and Assignees make no representation that these translations are complete or correct.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Mail Stop Amendment, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

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Michael W. Garvey  
Name of Attorney for Applicant(s)

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February 2, 2005  
Date

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Signature of Attorney

If there are any fees associated with this communication, please charge said fees to  
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Respectfully submitted,

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INFORMATION DISCLOSURE CITATION  
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APPLICANT:  
**Kazushi Higashi et al.**FILING DATE:  
**July 25, 2003**GROUP ART UNIT:  
**4217**

## U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Subclass	Filing Date
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						

## FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subclass	Translation
	I	3-241755	10/1991	JP			Eng. abstract & Partial Trans. Attached
	J						

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	K	"Development of chip-on-chip bonding process at a room temperature (with copper, a bumpless bonding is also possible)", Semiconductor Sangyo Newspaper, June 12, 2002, pg. 9, Sangyo Times Inc., Tokyo, Japan.
	L	"Development of chip-on-chip bonding process at a room temperature by a superbonder", Electronic Materials, July 1, 2002, pp. 8-9, Vol. 41 No. 7, Kogyo Chosakai Publishing Co., Ltd., Tokyo, Japan.
	M	"Ultrasonic Flip Chip Bonding Technology for LSI Chip with High Pin Counts" by Kajiwara et al., from Proceedings of the 7th Symposium on Microjoining and Assembly Technology in Electronics, February 1, 2001, pp. 16166, Japan Welding Society, Tokyo, Japan.
	N	

Examiner:

Date Considered

\*Examiner: Initial if reference considered, regardless of whether citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.